

UNIVERSITY OF GAZIANTEP
ELECTRICAL AND ELECTRONICS ENGINEERING DEPARTMENT
EEE 441 DIGITAL DESIGN II
LABORATORY EXPERIMENT 6
SEQUENTIAL CIRCUIT DESIGN USING FPGA - II

1 OBJECT

In this experiment you will design and implement a synchronous sequential circuit on FPGA by using Verilog HDL.

2 EXPERIMENTAL WORK

(E1) Design a 8-bit synchronous binary Up/Down counter using Verilog and implement your circuit on Atlys board. Circuit must have an up and down count mode input, a reset input and a count enable input. Connect these inputs to 3 switches and output of the counter to 8 leds on the Atlys board. Implement your circuit on ISE (generate programming file) and download the bitstream to FPGA. Verify that your circuit works correctly on the FPGA board.

3 User Constraints File (UCF)

This file is available as “AtlysGeneral.ucf” on the embedded systems laboratory. You can change signal names (NET) according to your design and use it. Do not modify LOC values. Below code is the UCF description for this experiment.

```
# clock pin for Atlys rev C board
NET "clk"  LOC = "L15"; # Bank = 1, Pin name = IO_L42P_GCLK7_M1UDM, Type = GCLK, Sch name = GCLK

# onboard Leds
NET "Led<0>" LOC = "U18"; # Bank = 1, Pin name = IO_L52N_M1DQ15, Sch name = LD0
NET "Led<1>" LOC = "M14"; # Bank = 1, Pin name = IO_L53P, Sch name = LD1
NET "Led<2>" LOC = "N14"; # Bank = 1, Pin name = IO_L53N_VREF, Sch name = LD2
NET "Led<3>" LOC = "L14"; # Bank = 1, Pin name = IO_L61P, Sch name = LD3
NET "Led<4>" LOC = "M13"; # Bank = 1, Pin name = IO_L61N, Sch name = LD4
NET "Led<5>" LOC = "D4"; # Bank = 0, Pin name = IO_L1P_HSWAPEN_0, Sch name = HSWAP/LD5
NET "Led<6>" LOC = "P16"; # Bank = 1, Pin name = IO_L74N_DOUT_BUSY_1, Sch name = LD6
NET "Led<7>" LOC = "N12"; # Bank = 2, Pin name = IO_L13P_M1_2, Sch name = M1/LD7

# onboard SWITCHES
NET "rst" LOC = "A10"; # Bank = 0, Pin name = IO_L37N_GCLK12, Sch name = SW0
NET "count" LOC = "D14"; # Bank = 0, Pin name = IO_L65P_SCP3, Sch name = SW1
NET "mode" LOC = "C14"; # Bank = 0, Pin name = IO_L65N_SCP2, Sch name = SW2
```