UNIVERSITY OF GAZIANTEP

ELECTRICAL AND ELECTRONICS ENGINEERING DEPARTMENT

EEE 441 DIGITAL DESIGN II

LABORATORY EXPERIMENT 4

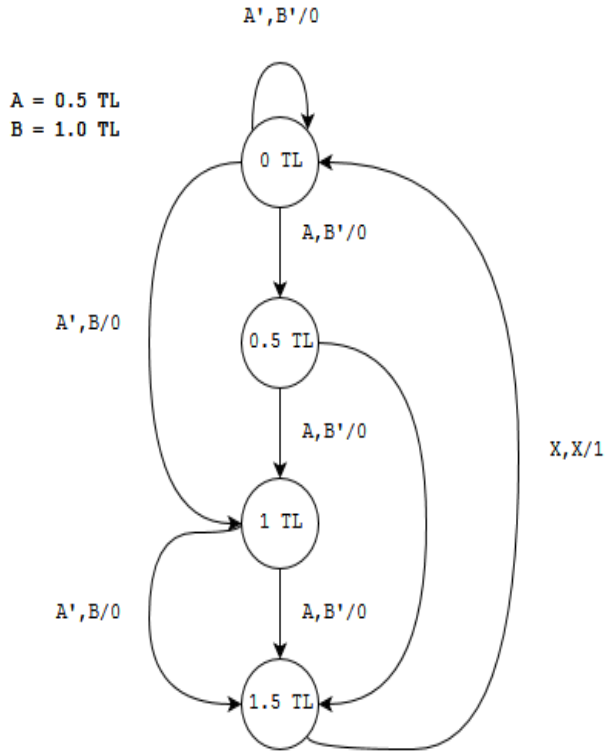
SEQUENTIAL CIRCUIT DESIGN USING FPGA - I

1.OBJECT

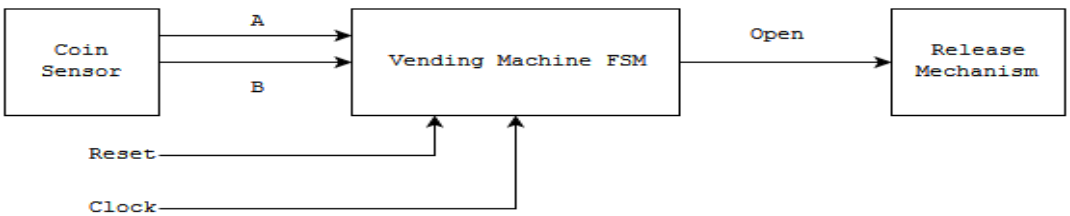
In this experiment you will design and simulate a synchronous sequential circuit by using Verilog HDL and Isim simulator.

2.EXPERIMENTAL WORK

E1. Design a FSM based Vending Machine controller using Verilog HDL and synthesize your circuit. State diagram and Truth Table of the controller is given below.



Present State	A	B	Next State	Open
0 TL	0	0	0 TL	0
	0	1	1 TL	0
	1	0	0.5 TL	0
	1	1	X	X
0.5 TL	0	0	0.5 TL	0
	0	1	1.5 TL	0
	1	0	1 TL	0
	1	1	X	X
1 TL	0	0	1 TL	0
	0	1	1.5 TL	0
	1	0	1.5 TL	0
	1	1	X	X
1.5 TL	X	X	0 TL	1



E2. Simulate the circuit you have designed in E1 using Isim logic simulator. Observe state transitions and output value. Create a testbench file in ISE and pick E1 as the "Unit Under Test" (UUT). Add the following code to the stimulus section of the testbench file.

```
rst = 1;

@(posedge clk) A = 1;

#100 @(posedge clk) A = 0;

B = 1;

#100 @(posedge clk) B = 0;


#100 @(posedge clk) A = 1;

#300 @(posedge clk) A = 0;


#100 @(posedge clk) B = 1;

#200 @(posedge clk) B = 0;
```

Also add, `initial forever #50 clk = ~clk;` line to simulate a 100 MHz clock signal.