UNIVERSITY OF GAZIANTEP

ELECTRICAL AND ELECTRONICS ENGINEERING DEPARTMENT

EEE 441 DIGITAL DESIGN II

LABORATORY EXPERIMENT 2

FPGA IMPLEMENTATION OF FLIP-FLOPS

1. OBJECT

In this experiment you will implement two basic flip-flops by using Verilog HDL.

2. EXPERIMENTAL WORK

E1. Write Verilog code for the D Flip-Flop with synchronous reset. Write and draw RTL Schematic (view using ISE) and HDL code on your laboratory notebook.

E2. Write Verilog code for the JK Flip-Flop with synchronous preset and clear. Write and draw RTL Schematic (view using ISE) and HDL code on your laboratory notebook.