

UNIVERSITY OF GAZIANTEP
ELECTRICAL AND ELECTRONICS ENGINEERING DEPARTMENT
EEE 441 DIGITAL DESIGN II
LABORATORY EXPERIMENT 1
FLIP-FLOPS

1. OBJECT

In this experiment you will construct and test the operation of various flip-flop circuits.

2. PRELIMINARY WORK

P1. The S-R latch is a basic flip-flop made with two cross coupled NAND gates. Draw its logic diagram and derive its truth table.

P2. Draw the logic diagram of a clocked RS flip-flop with four NAND gates.

P3. Consider a J--K' flip-flop , i.e, a J-K flip-flop with an inverter between external input K' and internal input K.

- Obtain the flip-flop characteristic table.
- Obtain the characteristic equation.
- Show that tying the two external inputs together forms a D flip-flop.

3. EXPERIMENTAL PROCEDURE

E1. Construct a basic flip-flop circuit with NAND gates. Connect the two inputs to switches and the two outputs to indicator lamps. Set the switches to logic 1, then momentarily turn each switch separately to logic 0 position and back to 1. Obtain the truth table of the circuit.

E2. Construct a clocked RS flip-flop with four NAND gates. Connect the S and R inputs to two switches and the clock input to a pulse generator. Verify the characteristic table of the flip-flop.

E3. In the clocked flip-flops (FFs), the R,S,J,K,T and D inputs have been referred to as control inputs. These inputs are also called synchronous inputs since their effect on the FF output is synchronized with the clock (CLK) input. Most clock FFs also have one or more asynchronous inputs which operate independently of the synchronous inputs and clock input. These asynchronous inputs can be used to set the FF to the 1 or clear the FF to the 0 state at any time regardless of the conditions at the other inputs. In a clocked J-K flip-flop two asynchronous inputs are designated as PRE (PRESET) and CLR (CLEAR). Investigate the operation of clocked J-K flip-flop and verify its function table given below.

E4. Investigate the operation of clocked D flip-flop and verify its function table.

Function Table for J-K Flip-Flop

INPUTS					OUTPUTS	
Preset	Clear	Clock	J	K	Q	Q'
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	1
1	1	P	0	0	No Change	
1	1	P	0	1	0	1
1	1	P	1	0	1	0
1	1	P	1	1	Toggle	

Function Table for D Flip-Flop

INPUTS				OUTPUTS	
Preset	Clear	Clock	D	Q	Q'
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1	1
1	1	P	0	0	1
1	1	P	1	1	0
1	1	0	X	No Change	

4. QUESTIONS

Q1. When power is first applied to any FF circuit, it is impossible to predict the initial state of Q and Q'. What could be done to ensure that a NAND latch always started off in the Q=1 state?

Q2. What J-K input condition will always set Q upon the occurrence of the active CLK transition?

Q3. Can a D flip-flop respond to its D and CLK inputs while PR=1?

Q4. List the conditions necessary for a positive edge trigger J-K flip-flop with active LOW asynchronous inputs to toggle to its opposite state.

Q5. List at least three common application of clocked flip-flop.

Q6. A 20kHz clock signal is applied to a JK flip flop with J=K=1. What is the frequency of the flip-flop output waveforms?