EXPERİMENT-3

TTL-CMOS LOGIC GATES

3.1 OBJECTIVE

To observe Voltage-transfer characteristics of TTL and CMOS NOT Gates.

3.2 THEORY

Transistor–transistor logic (TTL) is a logic family built from bipolar junction transistors. Its name signifies that transistors perform both the logic function and the amplifying function. Many TTL and CMOS logic gates are fabricated onto a single integrated circuit (IC).

Standard TTL circuits operate with a 5-volt power supply. A TTL input signal is defined as "low" when between 0 V and 0.8 V with respect to the ground terminal, and "high" when between 2 V and V_{CC} (5 V), and if a voltage signal ranging between 0.8 V and 2.0 V is sent into the input of a TTL gate, there is no certain response from the gate and therefore it is considered "uncertain" (precise logic levels vary slightly between sub-types and by temperature).

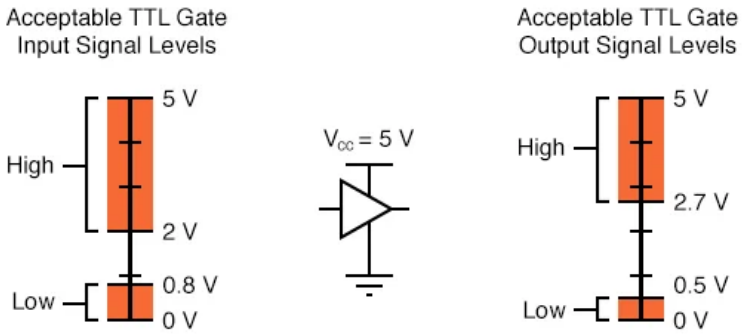


Figure 3.1

CMOS gate circuits have input and output signal specifications that are quite different from TTL. For a CMOS gate can operating at a power supply voltage range of 3-18 volts, For 5V voltage source, the acceptable input signal voltages range from 0 volts to 1.5 volts for a “low” logic state, and 3.5 volts to 5 volts for a “high” logic state. “Acceptable” output signal voltages (voltage levels guaranteed by the gate manufacturer over a specified range of load conditions) range from 0 volts to 0.05 volts for a “low” logic state, and 4.95 volts to 5 volts for a “high” logic state.:

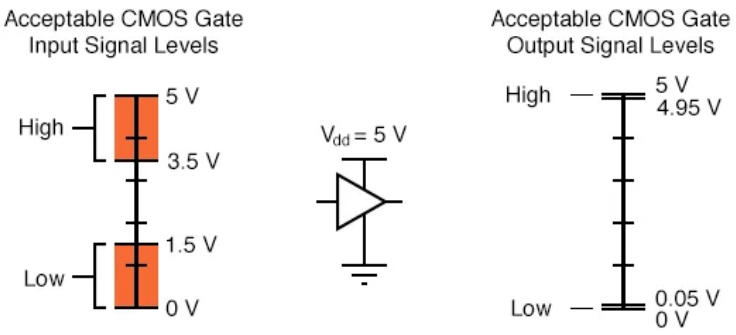


Figure 3.2.

The tolerable ranges for output signal levels are narrower than for input signal levels, to ensure that any gate outputting a digital signal into the input of another gate will transmit voltages acceptable to the receiving gate. The difference between the tolerable output and input ranges is called the noise margin of the gate. Noise must exceed noise margin to make second gate produce wrong output.

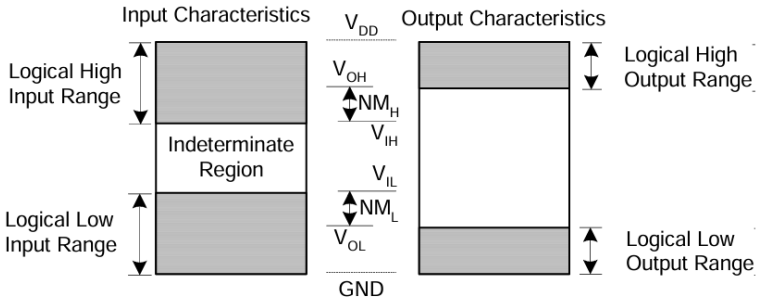


Figure 3.3. Noise Margins

V_{IL}: Maximum input voltage that is still a valid logic 0 at the input.

V_{IH}: Minumum input voltage that is still a valid logic 0 at the input.

V_{OL}: Maximum output voltage that will appear at the gate output when the output is supposed to be logic 0.

V_{OH}: Minumum output voltage that will appear at the gate output when the output is supposed to be logic 1.

NM_L: Low noise margin

NM_H: High noise margin

3.2.1 NOT GATE

In digital logic, an inverter or NOT gate is a logic gate which implements logical negation. It outputs are opposite of the bit that is put into it. The bits are typically implemented as two differing voltage levels. Symbol and the voltage transfer characteristic of a NOT gate are shown in figüre 3.4.

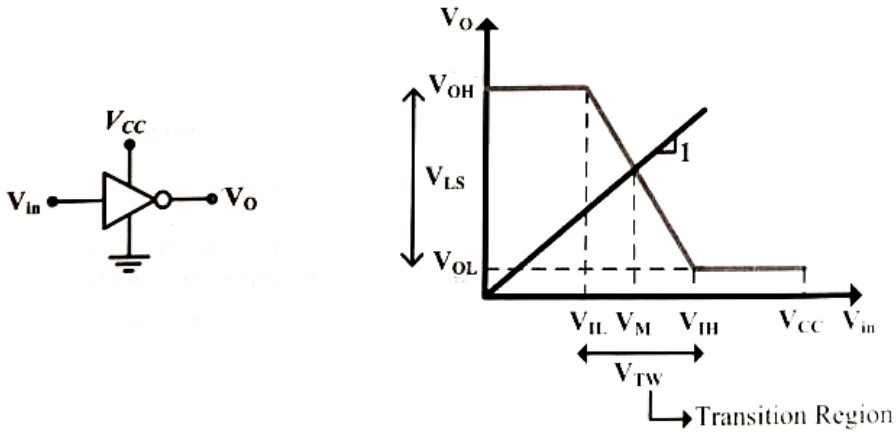


Figure 3.4. NOT Gate symbol and its Voltage Transfer Characteristic

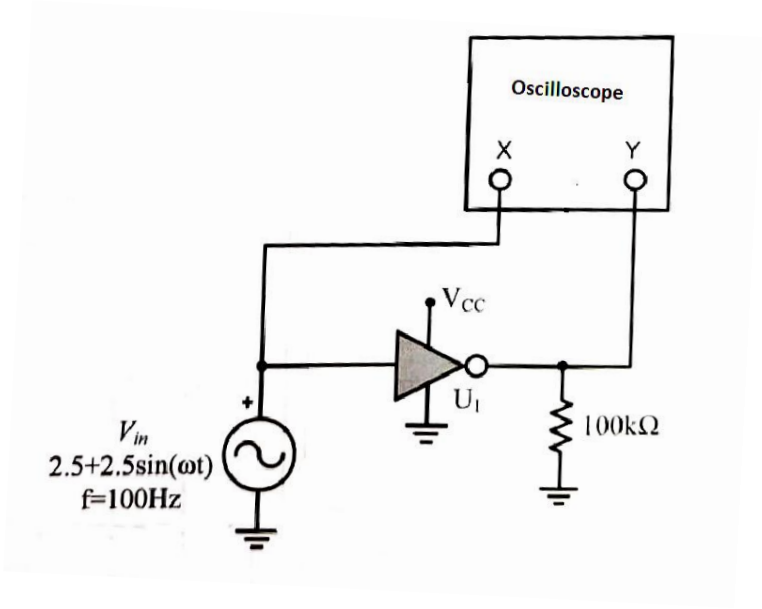
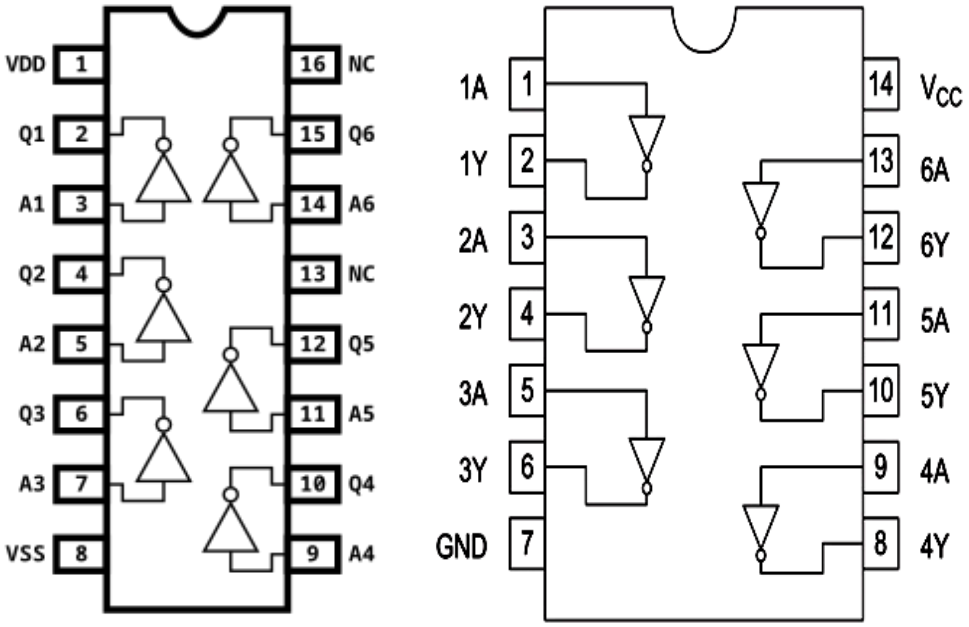


Figure 3.5. A Circuit to obtain voltage transfer characteristic of a gate



a) **b)**

Figure 3.6. a) 4049 CMOS NOT Gate and b) 74LS04 TTL NOT Gate

3.3 PRELIMINARY

3.3.1 Make a Pspice analysis (Run a DC sweep from 0V to 5V) of the circuit shown in Figure 3.5 and obtain voltage transfer characteristics of 74LS04 TTL NOT Gate and 4049 CMOS NOT Gate. **Bring these graph when you come to lab.**

3.3.2 Using the VTC of NOT Gates Find All Noise Margin parameters($V_{OH}, V_{OL}, V_{IH}, V_{IL}$) and Fill the table 3.1.

	74LS04	4049
V_{OH}		
V_{OL}		
V_{IH}		
V_{IL}		
NM_H		
NM_L		

Table 3.1

3.4 EXPERIMENTAL PROCEDURE

3.4.1 Connect the circuit as shown in Figure 3.5 with 74LS04 IC.

- $V_{CC} = 5V$
- Sketch the VTC of NOT Gates by using XY mode of oscilloscope.
- Using the VTC of NOT Gates, Find All Noise Margin parameters($V_{OH}, V_{OL}, V_{IH}, V_{IL}$) and Fill the table 3.2.
- Repeat all steps above for 4049 CMOS IC.

74LS04

4049

	74LS04	4049
V_{OH}		
V_{OL}		
V_{IH}		
V_{IL}		
NM_H		
NM_L		

Table 3.2

3.5 CONCLUSIONS

3.5.1 Compare the pspice and experimantal results. Is there any differences between them? Why?

3.6 EQUIPMENT LIST

- Resistors : 100kΩ
- ICs : 74LS04, CD4049
- Standart Set Equipment