EXPERİMENT - 4

DTL-TTL LOGIC GATES

4.1 OBJECTIVE

This experiment aims to explore and understand key characteristics of diode-transistor logic (DTL) circuits and transistor-transistor logic (TTL) circuit families.

4.2 THEORY

Logic gates can be categorized based on their logical functions or the type of logic families they belong to. An understanding of the physical capabilities and constraints of a logical element is crucial for successfully implementing any digital system. A logic family refers to the broader physical structure used to realize a logical element, such as TTL (Transistor-Transistor Logic), ECL (Emitter-Coupled Logic), or CMOS (Complementary Metal-Oxide Semiconductor) logic families. Each logic family encompasses one or more distinct logic series, each offering unique characteristics in comparison to others within the same family. For instance, the TTL logic family includes several series, such as the 74 standard, 74L (low-power), 74H (high-speed), 74S (standard Schottky), 74LS (low-power Schottky), and 74ALS (advanced low-power Schottky) series.

4.2.1 Basic DTL NOT Gate Circuit

The basic circuit of a DTL NOT gate and its voltage-transfer characteristic (VTC) are illustrated in Fig. 4.1. In the scenario where the transistor is cut off, $V_O = V_{OH} = V_{CC}$. Since the input diode of the load gate is reverse biased, only reverse or leakage current flows through the collector resistor R_C of the driving gate, making V_{OH} unaffected by the number of load gates connected to the output. When the transistor enters saturation, $V_O = V_{OL} = V_{CE(SAT)}$. The inverting transistor reaches the threshold of conduction when $V_{BE} = V_{BE(on)}$.

$$V_{IL} = V_{BE(on)} + 2V_{D(on)} - V_{D(on)} = V_{BE(on)} + V_{D(on)}$$

The inverting transistor reaches the threshold of simulation when $V_{BE} = V_{BE(sat)}$.

$$V_{IH} = V_{BE(sat)} + 2V_{D(on)} - V_{D(on)} = V_{BE(sat)} + V_{D(on)}$$

Logic swing is given as

$$\text{LS} = V_{OH} - V_{OL}$$

Noise margins

$$\text{N}M_H = V_{OH} - V_{IH}$$

$$\text{N}M_L = V_{IL} - V_{OL}$$

For low output, fan-out(N) can be written as

$$\text{Fan-out} = \text{N} = \frac{Total\ output\ current\ of\ gate}{Drive\ current\ for\ each\ smilar\ gate} = \frac{I_{LT}}{I_1}$$

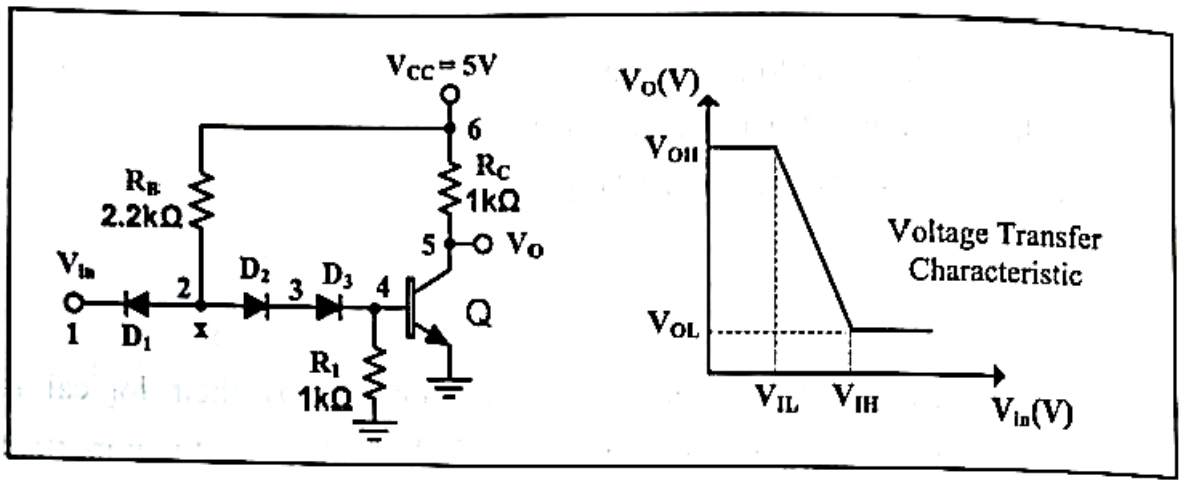


Figure 4.1 Basic DTL circuit and its voltage-transfer characteristic.

4.2.2 Basic TTL NOT Gate Circuit

The fundamental TTL NOT gate circuit is illustrated in Figure 4.2. When the input is at logic 0, transistor Q4 becomes forward-biased and enters the saturation region, while transistor Q5 remains in the cutoff region. $V_O = V_{CC}$= logic 1. Conversely, when the input is at logic 1, Q4 operates in the inverse active mode, and Q5 transitions to the saturation region. $V_O = V_{CE(sat)} = logic\ 0$.

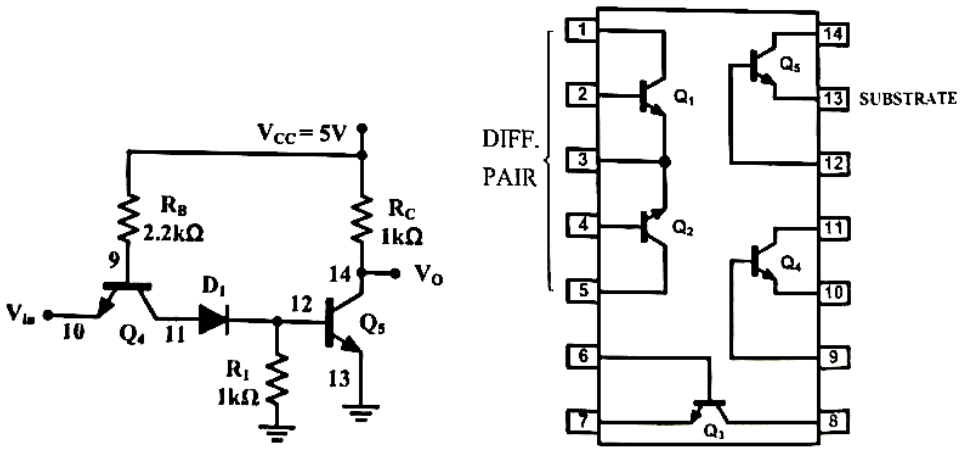


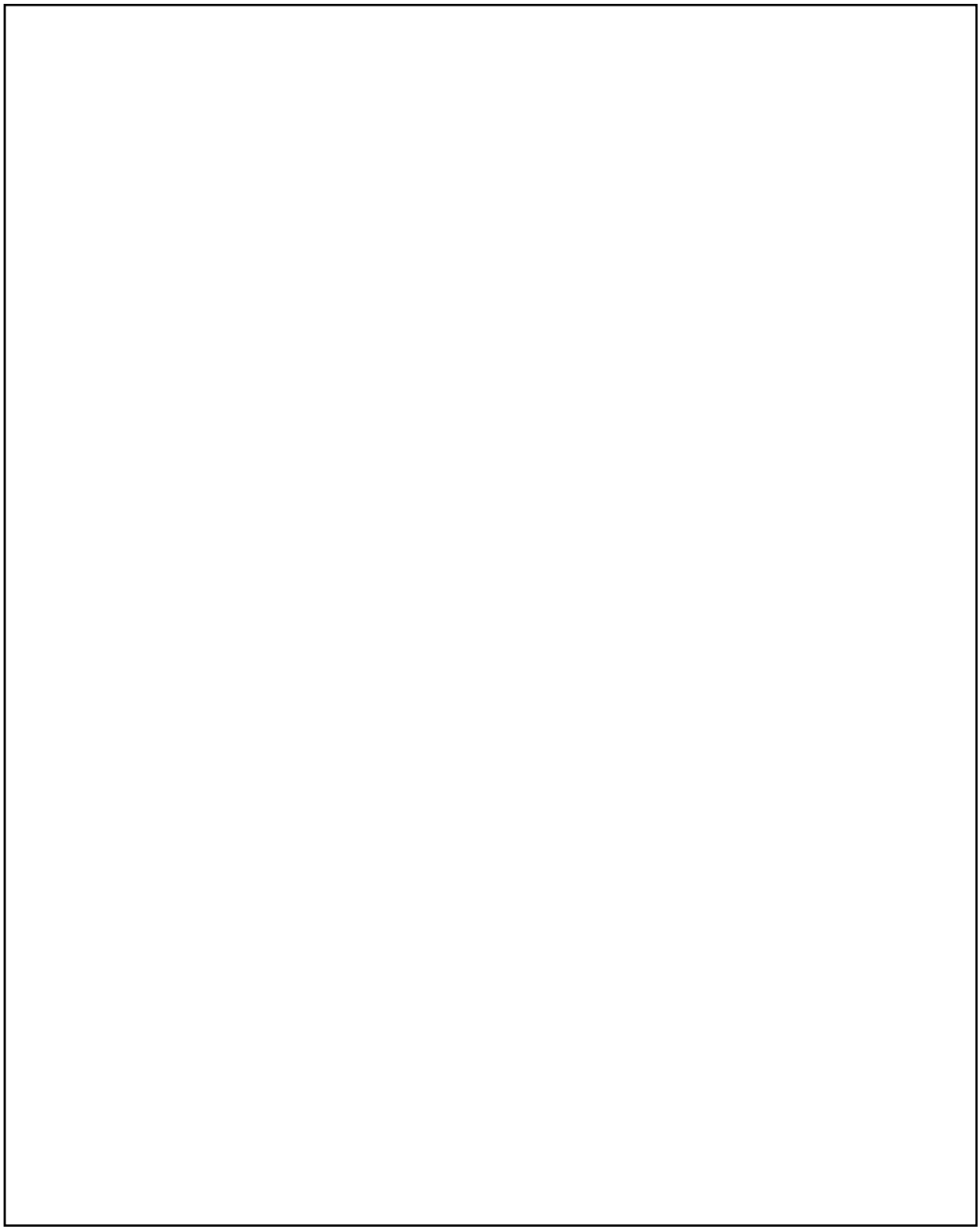
Figure 4.2 Basic TTL circuit and CA3146 IC.

4.3 PRELIMINARY

$V_{BE}(on) = V_D(on) = 0.7V, V_{BE}(sat) = 0.8V, V_{CE}(sat) = 0.2V, \beta$=100, $\beta_R = 0.1$.

4.3.1 For DTL circuit as shown in Figure 4.1,

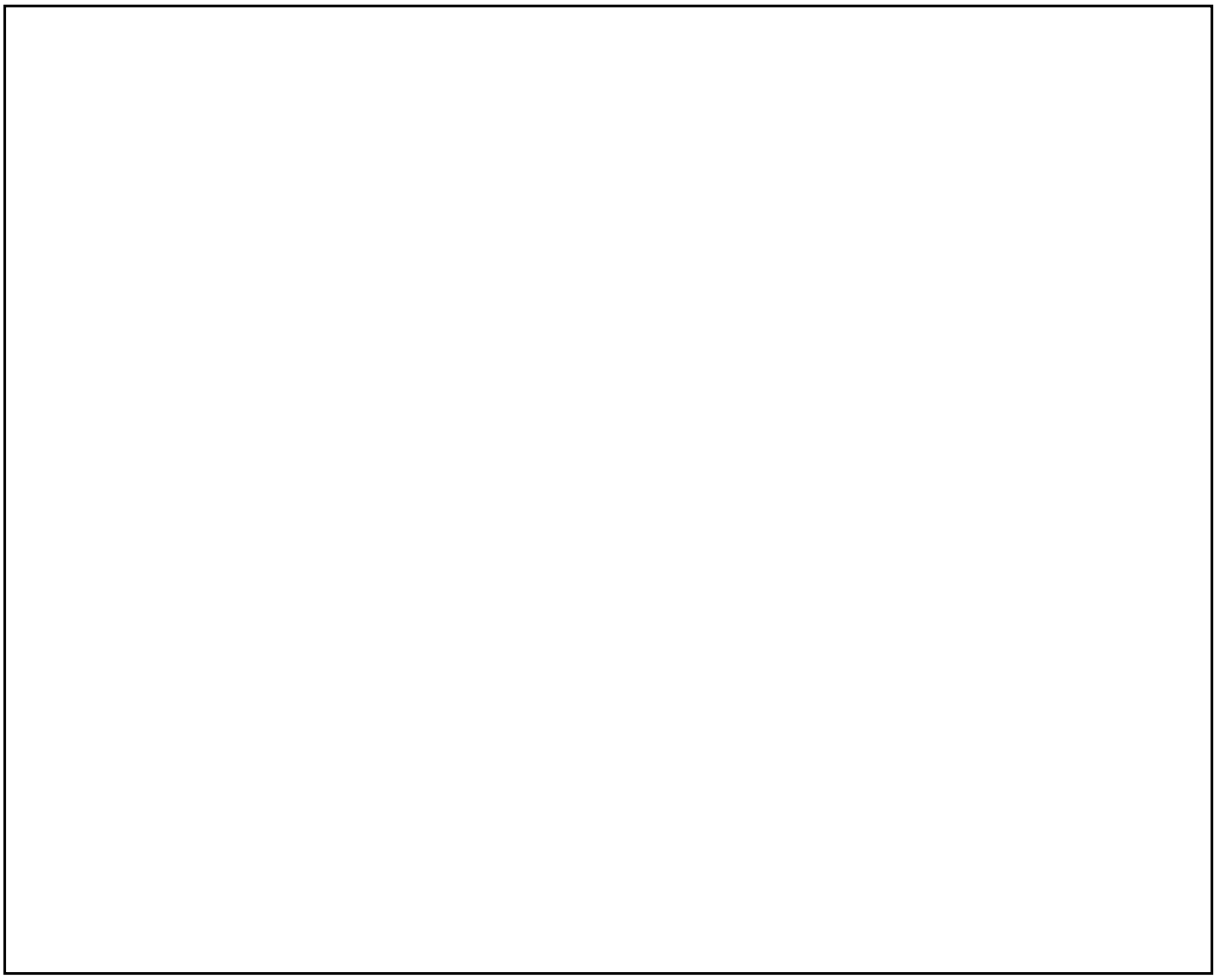
- Sketch the VTC,
- Find and replace $V_{OH}, V_{OL}, V_{IH}, V_{IL}$ and noise margins listed below.



	Calculated		PSpice		Experimental	
	DTL	TTL	DTL	TTL	DTL	TTL
V_{OH}						
V_{OL}						
V_{IH}						
V_{IL}						
NM_H						
NM_L						

Table 4.1

4.3.2 Repeat part(4.3.1) for TTL circuit given in Figure 4.2.



4.3.3 Perform a PSpice analysis (Run a DC sweep from 0V to 5V on the input V_{in}) of circuit shown in Figure 4.1. **Bring these graph when you come to lab.**

- Obtain $V_o - V_{in}$ voltage transfer characteristics(VTC) of the circuit.
- Using VTC, find and replace $V_{OH}, V_{OL}, V_{IH}, V_{IL}$ and noise margins listed in Table 4.1.

4.3.3 Repeat part (4.3.3) fort he circuit given in Figure 4.2.

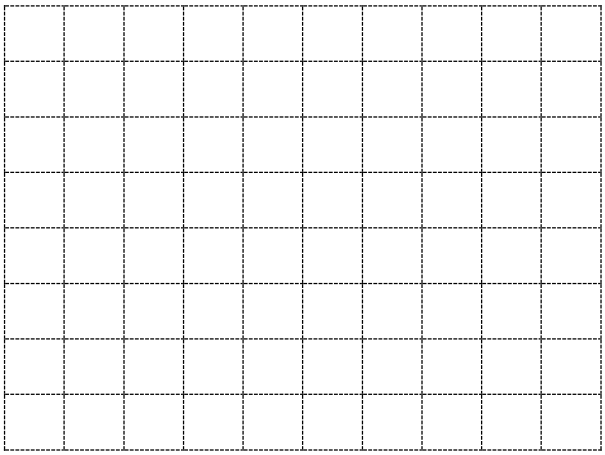
4.4 EXPERIMENTAL PROCEDURE

- $V_{in} = 2.5 + 2.5\sin(2\pi 100t)$.

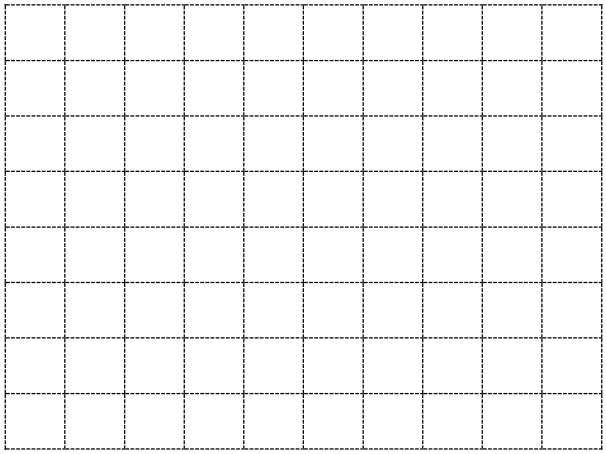
4.4.1 Setup the circuit as shown in Figure 4.1.

- Observe and plot the VTC.
- Find and replace $V_{OH}, V_{OL}, V_{IH}, V_{IL}$ and noise margins listed in table 4.1.

4.4.2 Repeat part(4.4.1) for TTL circuit given in Figure 4.2.



DTL



TTL

4.5 CONCLUSIONS

4.5.1 Analyze the findings from both the preliminary and experimental results, and identify any discrepancies between them. If differences are observed, provide an explanation for the underlying reasons.

4.6 EQUIPMENT LIST

- Resistors : 2.2kΩ, 4.7kΩ
- IC : CA3146
- Rectifier diodes : 3x1N4148
- Standart Set Equipment :