EXPERİMENT - 5

NMOS-CMOS INVERTERS

5.1 OBJECTIVE

The purpose of this experiment is to provide an understanding of some of the characteristics of NMOS and CMOS inverter circuits. In this experiment, we will study NMOS and CMOS not gates.

5.2 THEORY

Inverters are circuit that give an inverting output for an input, i.e., if input is high, output is low and vice versa. MOSFET is a voltage-controlled current device in which the voltage applied between gate and source controls the flow of current from drain to source. There are two types of MOSFETs: PMOS (current flow is due to holes) and NMOS(current flow due to electrons). There is another connection in MOSFET called Substrate or body that in PMOS connected to the most positive potential in the circuit and in NMOS connected to the most negative potential in the circuit.

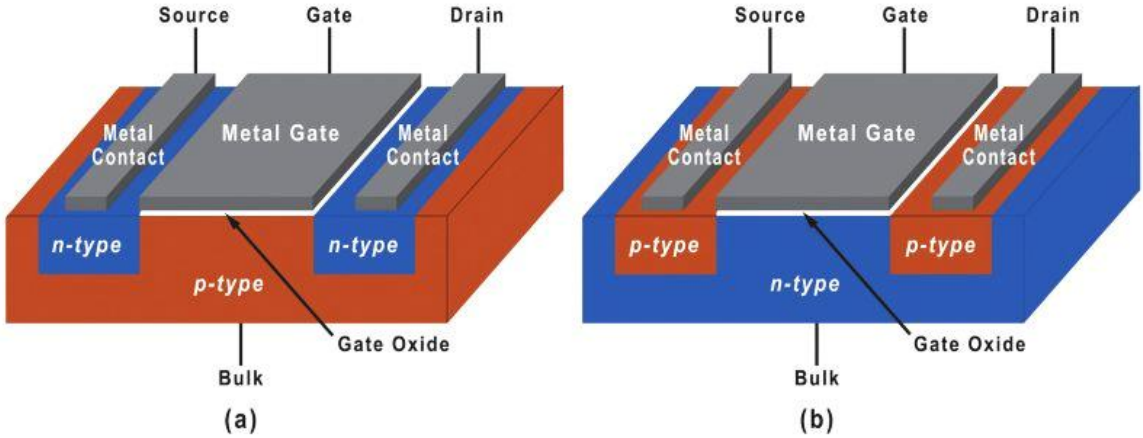


Figure 5.1 NMOS (a) and PMOS (b) MOSFETs.

MOSFET has three regions of operation: Linear (Triode), Saturation and Cutoff.

1. Cutoff Region

- **Condition**: $V_{GS} < V_{th}$
  - The MOSFET is off.
  - There is no significant current flow between the drain and source ($I_D \approx 0$).
  - The channel is not formed.

2. Linear (Triode) Region

- **Condition**: $V_{GS} > V_{th}$ and $V_{DS} < V_{GS} - V_{th}$
- **Behavior**:
  - The MOSFET operates like a variable resistor.
  - The drain current I_D is approximately linearly proportional to V_{DS}.
  - Current equation: $I_D = k_n [2(V_{GS} - V_{th}) V_{DS} - V_{DS}^2]$
  - where $k_n = \frac{\mu n Cox W}{L}$ is a process-dependent constant.

3. Saturation (Active) Region

- **Condition**: : $V_{GS} > V_{th}$ and $V_{DS} > V_{GS} - V_{th}$
- **Behavior**:
  - The MOSFET acts as a constant current source.

When V_{DS} *i*s further increased, I_D will no longer increase (until the breakdown) and it will become constant. The current n this region is given by the relation:

$$I_D(sat) = k_n(V_{GS} - V_{th})^2$$

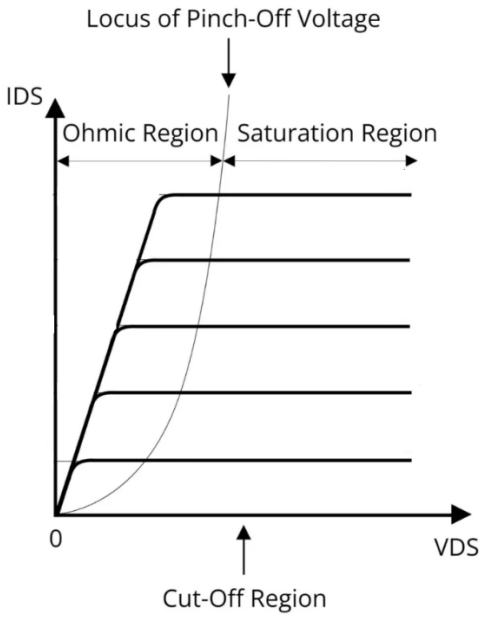


Figure 5.2 I-V Characteristics of an NMOS

MOSFET IC CD4007 that has 3 NMOSes and 3 PMOSes is used in the laboratory. The electrical symbols of enhancement mod NMOS and PMOS are given in Figure 5.3 and pin configuration of CD4007 is given in Figure 5.4.

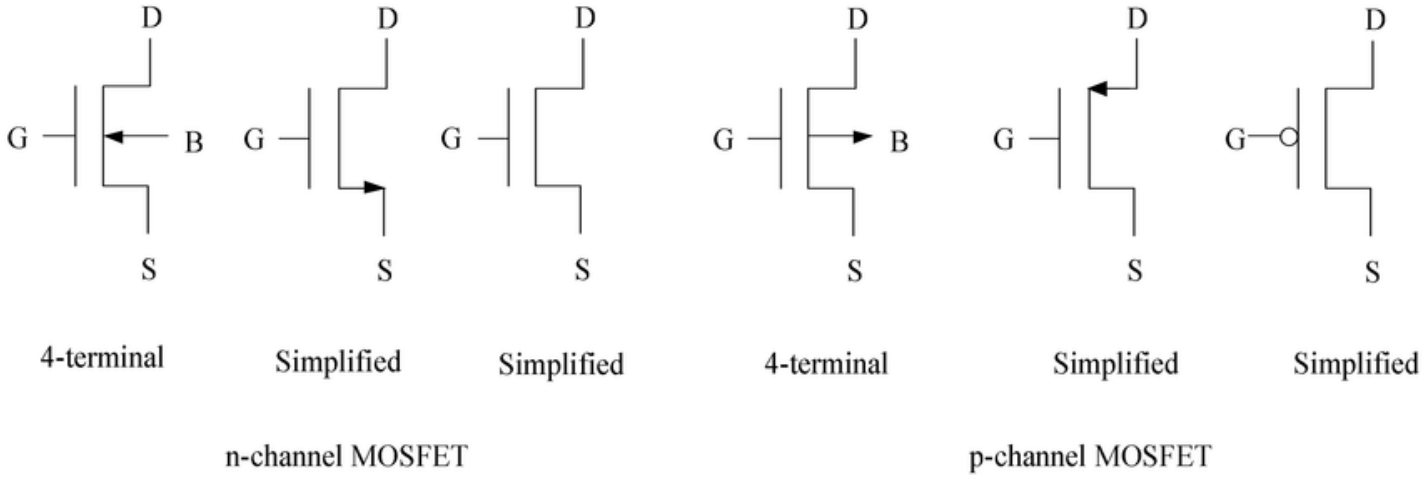


Figure 5.3 Electrical symbols for n-channel and p-channel enhancement type of MOSFETs.

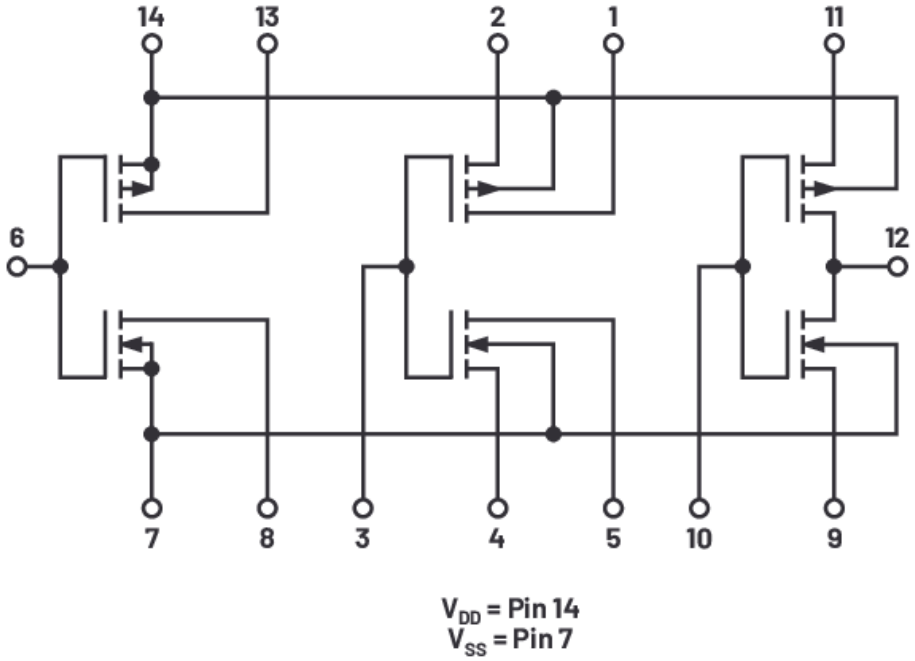
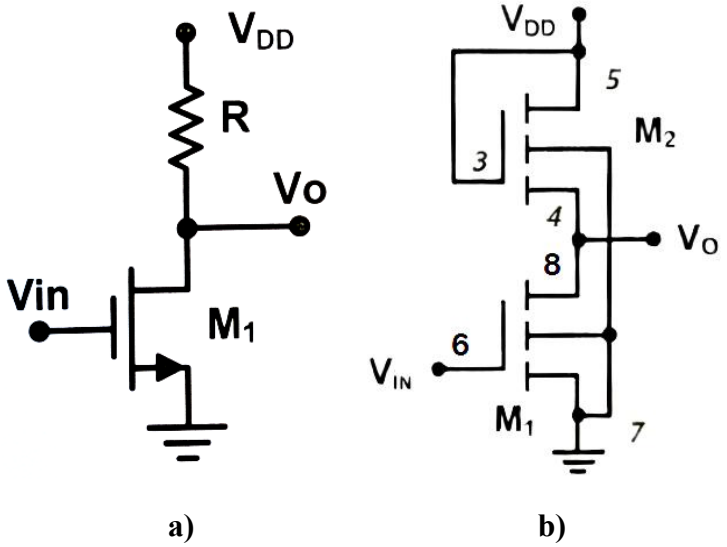


Figure 5.4 CD4007 Pin Configurations

5.2.1 MOS Inverter

The inverter circuits may be consructed with the n and p channel MOSFETs in the CD4007 MOS array chip. NMOS with resistive load is shown in Fİgure 5.3a. The inverter in shown Figure 3.5b is an NMOS-only inverter. In NMOS inverter M_1 acts as an inverter M_2 acts as active load, replacing the static resistor. Output logic low will never reach 0V for these inverters, and thus noise margins are poorer than the basic CMOS inverter. Also, DC power will be dissipated when the output logic level is a low since a drain current will flow through the inverters. A CMOS inverter is shown in Figure 5.6 Static power dissipation of a CMOS is zero.



a) **b)**

Figure 5.5 NMOS inverter with (a) resistive load (b) active load.

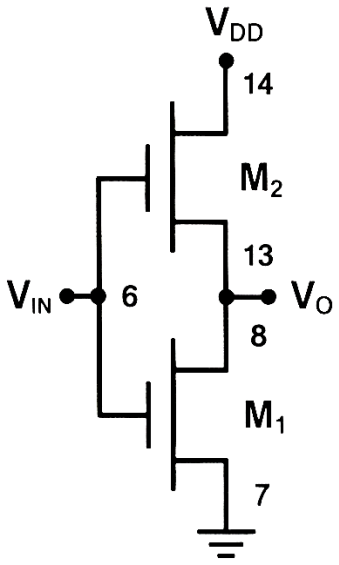


Figure 5.6 CMOS inverter

5.3 PRELIMINARY

R= 47kΩ and $V_{DD} = 5V$

k'=150 μA/V^2, $V_{th} = 1.2V, L = 2\mu m, W = 10\mu m, \lambda = 0\ for\ NMOS$

k'=75 μA/V^2, $V_{th} = -1.0V, L = 2\mu m, W = 20\mu m, \lambda = 0\ for\ PMOS$

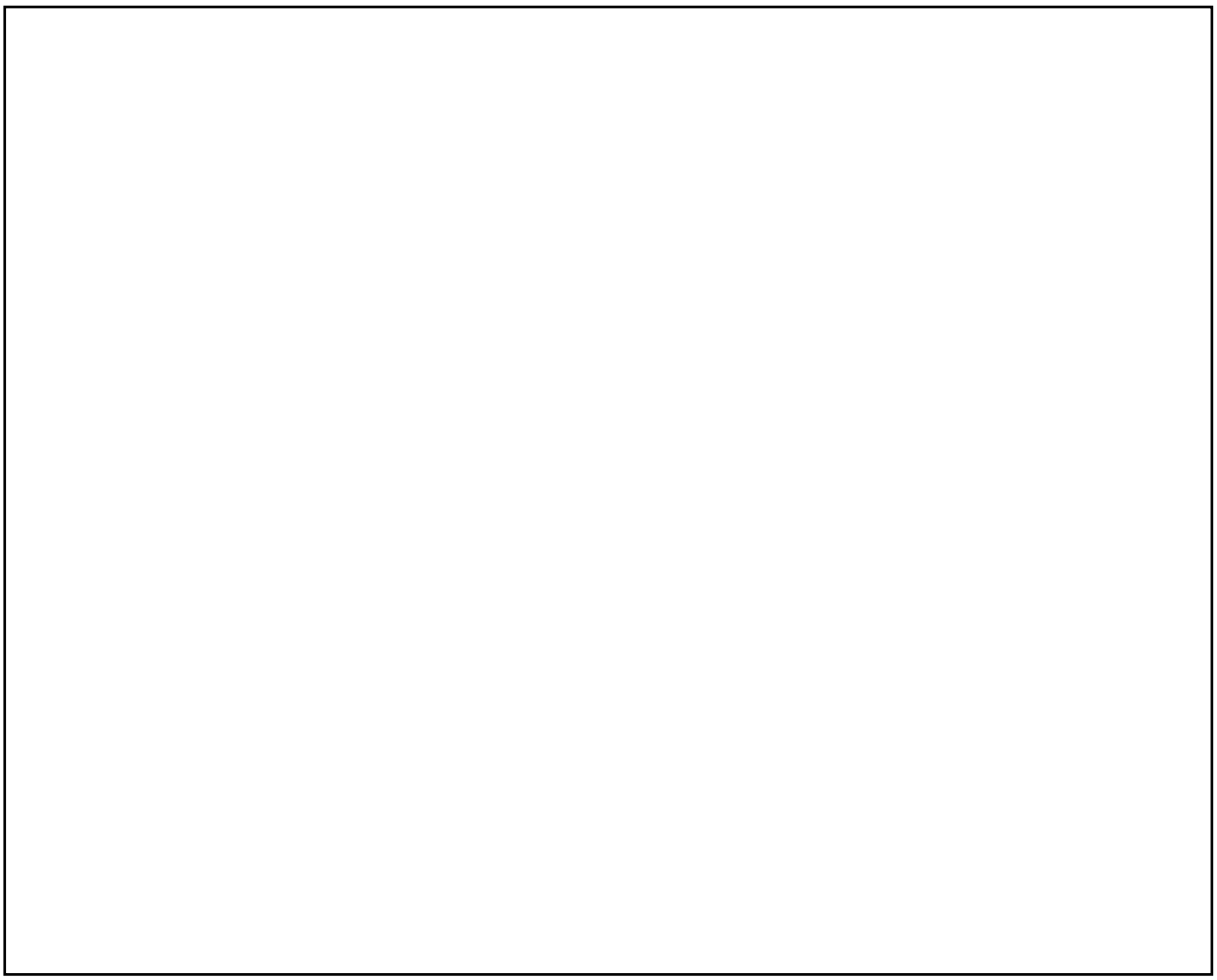
5.3.1 For NMOS circuit as shown in Figure 3.5a,

- Sketch the VTC
- Find and replace $V_{OH}, V_{OL}, V_{IH}, V_{IL}$ and noise margins listed in Table 5.1.

	Calculated		PSpice			Experimental		
	5.5a	5.6	5.5a	5.5b	5.6	5.5a	5.5b	5.6
V_{OH}								
V_{OL}								
V_{IH}								
V_{IL}								
NM_H								
NM_L								

Table 5.1

5.3.2 Repeat part(5.3.1) for the circuit given in Figure 5.6.

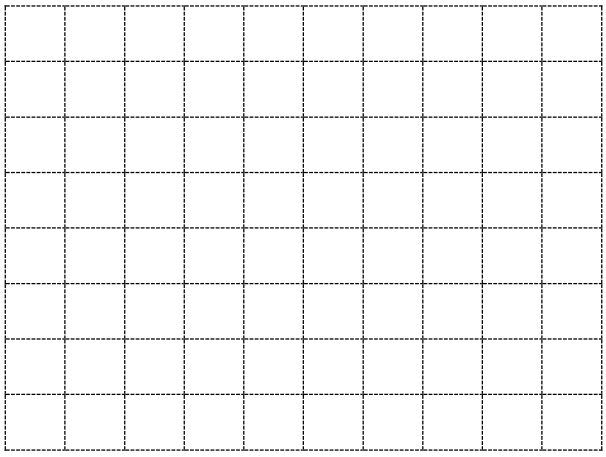


5.3.3 Perform a PSpice analysis (Run a DC sweep from 0V to 5V on the input V_{in}) of circuit shown in Figure 5.5a.

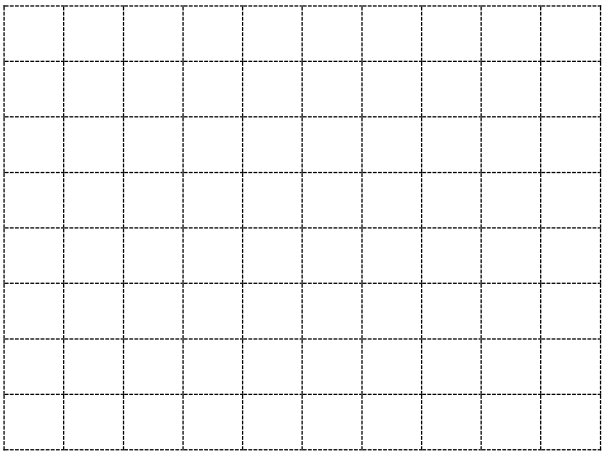
- Obtain $V_o - V_{in}$ voltage transfer characteristics(VTC) of the circuit.
- Using VTC, find and replace $V_{OH}, V_{OL}, V_{IH}, V_{IL}$ and noise margins listed in Table 5.1.

5.3.4 Repeat part(5.3.3) for the circuit given in Figure 5.5b.

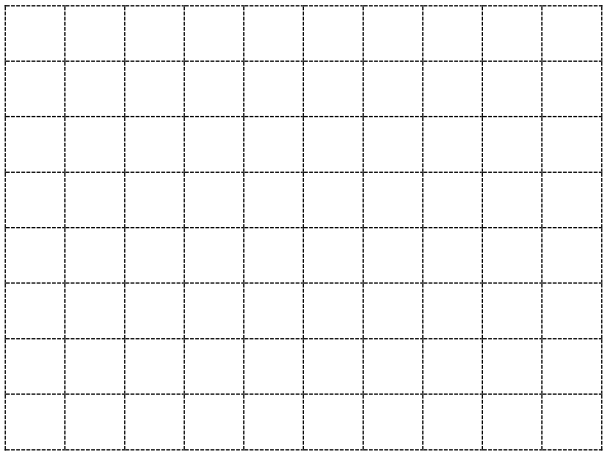
5.3.5 Repeat part(5.3.3) for the circuit given in Figure 5.6.



5.5a



5.5b



5.6

5.4 EXPERIMENTAL PROCEDURE

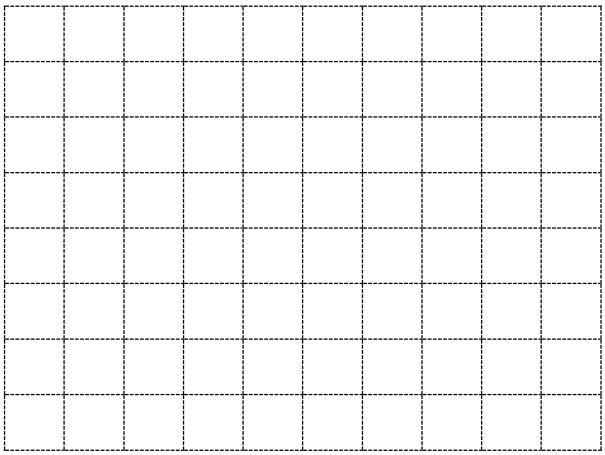
$V_{in} = 2.5 + 2.5\sin(2\pi 100t)$, R= 47kΩ and $V_{DD} = 5V$

5.4.1 Setup the circuit as shown in Figure 5.5a.

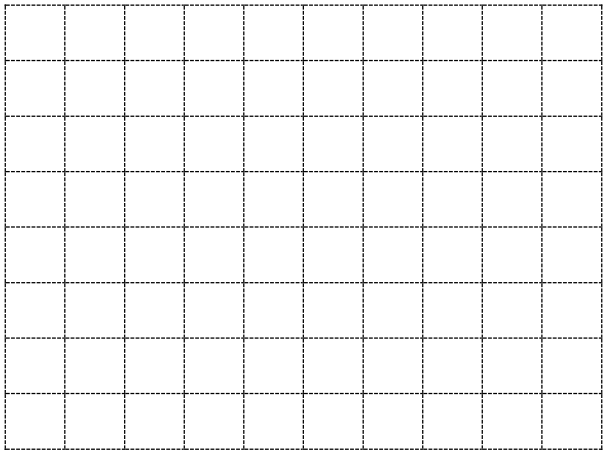
- Observe and plot the VTC.
- Find and replace $V_{OH}, V_{OL}, V_{IH}, V_{IL}$ and noise margins listed in table 5.1.

5.4.2 Repeat part(5.4.1) for the circuit given in Figure 5.5b.

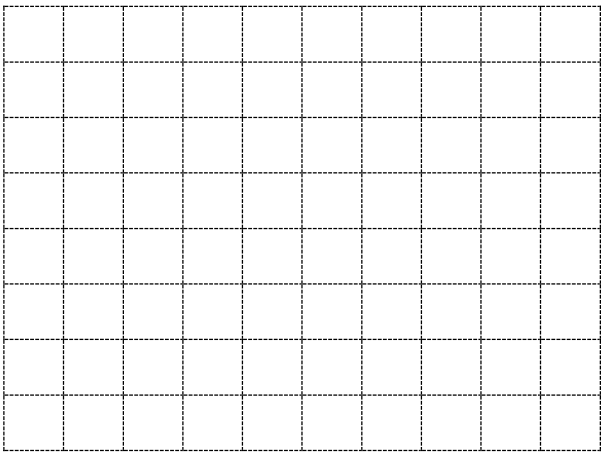
5.4.3 Repeat part(5.4.1) for the circuit given in Figure 5.6.



5.5a



5.5b



5.6

5.5 CONCLUSIONS

5.5.1 Compare the results obtained in the preliminary and experimantal results. If there exist some differences, explain the reasons.

5.6 EQUIPMENT LIST

- Resistors : 47kΩ
- IC s : CD4007
- Standart Set Equipment